**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | |
|---|---|
| Application No.: | 10/614,403 |
| Filing Date: | 07/07/2005 |
| Applicant: | Eitan Rosen |
| Group Art Unit: | 2138 |
| Examiner: | Saqib J. Siddiqui |
| Title: | INTEGRATED CIRCUIT TEST USING CLOCK SIGNAL MODIFICATION |
| Attorney Docket: | MP0278 |

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

**PRE-APPEAL BRIEF REQUEST FOR REVIEW AND PETITION FOR EXTENSION OF TIME**

Applicant requests a Pre-Appeal Brief Conference and contend that the combination of Dunn et al. (U.S. Pat. No. 6,463,570) and Sunter et al. (U.S. Pat. No. 6,204,694) fails to show, teach, or suggest the elements of the presently pending claims.

Applicant hereby petitions under the provisions of 37 C.F.R. § 1.136(a) for an extension of time in which to respond to the outstanding Office Action and includes a fee as set forth in 37 C.F.R. § 1.17(a) with this response for such extension of time.

## STATUS OF CLAIMS

Claims 1-8, 12-20, 24-31, 35-42, 46-53, 57-64, 68-75, 79-86, and 90 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dunn et al. (U.S. Pat. No. 6,463,570) and further in view of Sunter et al. (U.S. Pat. No. 6,204,694). This rejection is respectfully traversed.

## SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites an apparatus for testing an integrated circuit that includes a plurality of clocked storage elements interconnected by a plurality of signal paths. A signal generator changes a duration of selected pulses of a first clock signal to a second duration to produce a second clock signal. An analysis circuit **identifies one of the signal paths interconnecting the clocked storage elements as flawed based on the change of the duration to the second duration**.

Independent claims 13, 25, 36, 47, 58, 69, and 80 recite similar subject matter. For example, claim 13 recites analysis means for identifying one of the signal paths interconnecting the clocked storage elements as flawed based on the change of the duration to the second duration. Claim 25 recites a method including the step of identifying one of the signal paths as flawed based on the change of the duration to the second duration. Claim 36 recites a computer program that includes identifying one of the signal paths as flawed based on the change of the duration to the second duration. Claims 47, 58, 69, and 80 include subject matter analogous to claims 1, 13, 25, and 36, respectively.

## ARGUMENT

With respect to claim 1, as best understood by Applicant, Dunn, either singly or in combination with Sunter, fails to at least show, teach, or suggest changing a pulse duration of a first clock signal to a second duration to produce a second clock signal and identifying one of a plurality of signal paths interconnecting a plurality of clocked storage elements as flawed based on the change of the duration to the second duration. Instead, Dunn appears to disclose identifying faulty wafer regions.

The present invention is directed to testing clocked storage elements that are interconnected by signal paths. For example, "circuit 202 comprises a plurality of clocked storage elements such as flip-flops that are interconnected by a plurality of signal paths...Each clocked storage element comprises a clock input to receive a clock signal." (Paragraph [0028]). As shown in an exemplary embodiment in FIG. 2 of the present application, an analysis circuit 214 indicates one of the signal paths as flawed as described in Paragraph [0049]. (Please see Page 3 of the Response filed February 19, 2007, hereinafter "the Response").

The Examiner acknowledges that Sunter fails to disclose this limitation. Instead, the Examiner relies on Dunn to disclose an analysis circuit that identifies one of the signal paths as flawed. Applicant respectfully notes that Dunn still fails to make up for the deficiencies of Sunter and instead discloses identifying faulty wafer regions (i.e. layers). (Please see Pages 3-4 of the Response).

In contrast, Dunn discloses that ring oscillators are used to detect salicide layer imperfections (See Dunn, Column 3, Line 65 through Column 4, Line 2). Imperfections in a particular salicide layer result in a period change in an output signal of a

corresponding ring oscillator. The salicide layers are not signal paths between clocked storage elements.

Further, claim 1 recites **changing the duration of m selected pulses to a second duration** and identifying one of the signal paths as flawed **based on the change of the duration** to the second duration. In contrast, Dunn discloses that **a change in period of the ring oscillators indicates** a flawed salicide layer. Claim 1 is directed to deliberately changing a specific pulse duration, and identifying a flawed signal path based on a failure **caused by** the changed duration. The alleged combination fails to disclose this structure.

In the FINAL Office Action mailed May 8, 2007, the Examiner maintains that a particular die region can be interpreted as a signal path because "a die can comprise at least two points through which a signal is being propagated." (See Page 3, Lines 3-6 of the Office Action). The Examiner further alleges that, therefore, identifying a faulty die is equivalent to identifying a faulty signal path.

Applicant respectfully disagrees and notes that claim 1 recites that the signal paths are, specifically, signal paths that interconnect a plurality of clocked storage elements. In contrast, notwithstanding the Examiner's interpretation, Dunn still fails to disclose identifying a particular flawed signal path between clocked storage elements as claim 1 recites. Applicant notes that **identifying an entire die region as faulty is not analogous to specifically identifying a flawed signal path between clocked storage elements**.

Further, Applicant again notes that the present application is directed to **intentionally changing pulse durations of a first clock signal to produce a second**

**clock signal to identify flawed signal paths**. As described above and throughout Dunn (including FIG. 3A and Column 5, Line 50 through Column 6, Line 15), a ring oscillator is provided on each die. The ring oscillator is operated and measured to determine whether its period is within pre-selected screening limits. In other words, deviation of the frequency from a pre-selected frequency indicates whether the die is faulty. Applicant notes that this structure is in direct contradiction to Applicant's claim, which recites **actively changing the frequency of selected pulses and identify flawed signal paths based on this change**. Measuring an undesired frequency deviation is not analogous to intentionally changing the pulse duration of a first clock signal to produce a second clock signal.

Applicant respectfully submits that the combination fails to show, teach, or suggest i) changing duration of selected pulses of a first clock signal to produce a second clock signal to ii) identify a signal path that interconnects clocked storage elements as flawed. Accordingly, Applicant respectfully submits that the presently pending claims are in condition for allowance.

Respectfully submitted,

Dated: September 13, 2007

By: _____
Michael D. Wiggins, Reg. No. 34,764
Damian M. Aquino, Reg. No. 54,964

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. Box 828
Bloomfield Hills, Michigan 48303
(248) 641-1600

MDW/dma